AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (canceled).

2. (canceled).

3. (currently amended): A method for recovering a clock signal from an input data signal in a telecommunications system, the method comprising:

comparing said input data signal with a recovered clock signal in order to control a recovered clock signal generation;

generating a plurality of delayed clock signals, obtained by multi-delaying at least a reference signal, said delayed clock signals being phase-shifted with respect to each other;

selecting said recovered clock signal among said delayed clock signals;

employing a number of delayed signals, such that a sum of shifts associated with said delayed signals covers a bit period of said input data signal; and

~~The method according to claim 1, further comprising~~ dynamically changing ~~the~~ said number of delayed signals by comparing ~~the~~ said bit period with ~~the~~ said shift sum~~.~~;

wherein said delayed clock signals show a phase shift with respect to each other, that is nominally constant in time.

4. (currently amended): The method according to claim 3, wherein ~~the~~ a shift between each adjacent pair of delayed signals is nominally equal.

5. (previously presented): The method according to claim 3, further comprising obtaining said plurality of delayed clock signals by multi-delaying a single sole reference signal.

6. (currently amended): The method according to claim 4, further comprising selecting a first recovery signal and a second recovery signal before selecting ~~the~~ said recovery clock signal.

7. (currently amended): The method according to claim ~~5~~6, further comprising switching between said first recovery signal and said second recovery signal for selecting ~~the~~ said recovery clock signal.

8. (currently amended): The method according to claim ~~5~~6, further comprising shifting ~~the~~ said first recovery signal and ~~the~~ said second recovery signal by one time interval.

9. (currently amended): The method according to claim ~~6~~7, further comprising shifting ~~the~~ said first recovery signal and ~~the~~ said second recovery signal by one time interval.

10. (currently amended): The method according to claim ~~5~~6, further comprising providing enabling signals for activating switching between said first recovery signal and said second recovery signal.

11. (canceled).

12. (currently amended): A method for recovering a clock signal from an input data signal in a telecommunications system, the method comprising:

comparing said input data signal with a recovered clock signal in order to control a recovered clock signal generation;

generating a plurality of delayed clock signals, obtained by multi-delaying at least a reference signal, said delayed clock signals being phase-shifted with respect to each other;

selecting said recovered clock signal among said delayed clock signals;

employing a number of delayed signals, such that a sum of shifts associated with said delayed signals covers a bit period of said input data signal;

performing a comparison operation which includes comparing said input data signal with said recovered clock signal, by using a comparison of several phases of at least one of said input data signal and said recovered clock signal, so as to obtain a plurality of samples for each sampling cycle; and

~~The method according to claim 10, further comprising~~ filtering ~~the~~ an output of ~~the~~ said comparison operation~~.~~;

wherein said delayed clock signals show a phase shift with respect to each other, that is nominally constant in time.

13. (canceled).

14. (canceled).

15. (currently amended): A circuit for recovering a clock signal from an input data signal in a telecommunications network, comprising:

a generating means configured to generate a recovery clock signal; and

a phase comparator configured to compare said input data signal phase and said recovery clock signal phase for supplying a phase information, which controls said generating means of said recovery clock signal; and

a selection means;

wherein said generating means further comprises a delay line having a plurality of taps for generating a plurality of delayed signals;

wherein a sum of shifts associated with said delayed signals covers a bit period of said input data signal; and

~~The circuit according to claim 13, further comprising a selection means,~~ wherein said selection means comprises:

a selection block for selecting a first recovery signal and a second recovery signal from ~~the~~ said plurality of delayed signals~~,~~; and ~~further comprises~~

a switch block for switching between said first recovery signal and said second recovery signal.

16. (canceled).

17. (currently amended): A circuit for recovering a clock signal from an input data signal in a telecommunications network, comprising:

a generating means configured to generate a recovery clock signal; and

a phase comparator configured to compare said input data signal phase and said recovery clock signal phase for supplying a phase information, which controls said generating means of said recovery clock signal;

wherein said generating means further comprises a delay line having a plurality of taps for generating a plurality of delayed signals;

wherein a sum of shifts associated with said delayed signals covers a bit period of said input data signal;

wherein said generating means comprises a selection means of said recovered clock signal;

wherein said selection means further comprises a control logic driving a selection block and a switch block according to said phase information supplied by said phase comparator; and

~~The circuit according to claim 15,~~ wherein said control logic comprises a filter for filtering ~~the~~ said phase information.

18. (currently amended): A circuit for recovering a clock signal from an input data signal in a telecommunications network, comprising:

a generating means configured to generate a recovery clock signal; and

a phase comparator configured to compare said input data signal phase and said recovery clock signal phase for supplying a phase information, which controls said generating means of said recovery clock signal;

wherein said generating means further comprises a delay line having a plurality of taps for generating a plurality of delayed signals;

wherein a sum of shifts associated with said delayed signals covers a bit period of said input data signal;

wherein said generating means comprises a selection means of said recovered clock signal;

wherein said selection means further comprises a control logic driving a selection block and a switch block according to said phase information supplied by said phase comparator; and

~~The circuit according to claim 15,~~ wherein said control logic comprises a logic machine issuing selection signals and enable signals according to ~~the~~ said phase information.

19. (currently amended): A circuit for recovering a clock signal from an input data signal in a telecommunications network, comprising:

a generating means configured to generate a recovery clock signal;

a phase comparator configured to compare ~~the~~ said input data signal phase and ~~the~~said recovery clock signal phase for supplying a phase information, which controls said generating means of said recovery clock signal;

a selection means;

wherein said generating means comprises a delay line having a plurality of taps for generating a plurality of delayed signals;

wherein said selection means comprises a selection block for selecting a first recovery signal and a second recovery signal from ~~the~~ said plurality of delayed signals, and further comprises a switch block for switching between said first recovery signal and said second recovery signal.

20. (currently amended): The circuit according to claim ~~19~~22, wherein said control logic comprises a filter for filtering the phase information.

21. (currently amended): The circuit according to claim ~~19~~22, wherein said control logic comprises a logic machine issuing selection signals and enable signals according to the phase information.

22. (new): The circuit according to claim 19, further comprising a control logic configured to drive said selection block and said switch block according to said phase information supplied by said phase comparator.